

We claim:

- 1 1. A method of fabricating a reconfigurable processor for running moderately
2 complex programming applications comprising:
 - 3 (a) providing source code for a programming application,
 - 4 (b) entering the source code in a control flow graph generating compiler
5 to produce a control data flow graph of data flow control flow and branch points,
 - 6 (c) extracting from the control flow graph basic blocks of code lying
7 between branch points,
 - 8 (d) from the code lying between the branch points generating
9 intermediate data flow graphs,
 - 10 (e) identifying clusters shared among dfgs at the highest level of
11 granularity,
 - 12 (f) from the identified clusters determine the largest common subgraph
13 shared among the dfgs,
 - 14 (g) scheduling the largest common subgraph for fast accomplishment of
15 operations in the lcs, and
 - 16 (h) apply the scheduled lcs to the intermediate flow graphs replacing the
17 unscheduled lcs therein,
 - 18 (i) scheduling the intermediate flow graphs containing the lcs's for fast
19 accomplishment of operations in the intermediate flow graphs to derive data patches having
20 operations and timings of each intermediate flow graph,
 - 21 (j) combining the data patches to include operations and timing of the
22 lcs with operations and timings of each intermediate subgraph that are outside the lcs,
 - 23 (k) from the combined data patches scheduling for process time
24 reduction multiple uses of the lcs operations and timings necessary to accomplish
25 operations and timings of all intermediate subgraph employing the lcs, and
 - 26 (l) implementing in hardware having mixed granularities the operations
27 and timing of the lcs including:
 - 28 (i) partitioning,
 - 29 (ii) placing, and
 - 30 (iii) interconnection routing.

1 2. In a method of making an integrated circuit for use as a hardware
2 implemented part of a programmed operation implemented in software and hardware; the
3 improvement comprising identifying hardware circuit elements for execution of a largest
4 common subgraph common among a set of flow graphs representing the programmed
5 operation; partitioning into blocks the circuit elements; arranging the blocks on an area
6 representative of an available area of a surface of a substrate on which the circuit elements
7 are to be formed; routing interconnections among the blocks; partitioning into sub-blocks
8 the circuit elements of each block; arranging each sub-block on an area representative of
9 the block form which it has been partitioned routing interconnections among the sub-blocks
10 and iteratively partitioning and routing among lesser sub-blocks until the individual circuit
11 elements have been placed and routed.

1 3. The method according to claim 2, wherein the steps of routing comprise
2 locating conductors and switches for interconnections among blocks, sub-blocks and circuit
3 elements.

1 4. The method according to claim 3, wherein locating conductors and switches
2 further comprises locating variable switches to effect variable conductive paths among the
3 blocks, sub-blocks and circuit elements.

1 5. A method of scheduling process elements of hardware implementing a
2 software application, comprising:
3 (a) developing a control data flow graph from the software;
4 (b) using a first, non-exhaustive scheduling algorithm to relatively
5 quickly arrive at a first scheduling of the process elements;
6 (c) using a second more exhaustive scheduling algorithm for at least one
7 and less than all selected paths of the control data flow graph to reduce the time of
8 execution thereof; and
9 (d) once all paths of the control data flow graph have been scheduled,
10 including all of the second more exhaustive scheduling, merge all of schedules, respecting
11 data and resource dependencies.

1 6. The method of scheduling according to claim 5, wherein step (a) comprises
2 PCP scheduling.

1 7. The method of scheduling according to either claim 5 or 6, wherein step (b)
2 comprises branch and bound based scheduling.

1 8. A dedicated integrated circuit for performing the software operation having
2 processing elements scheduled according to claim 5.

1 9. A dedicated integrated circuit for performing the software operation having
2 processing elements scheduled according to claim 6.

1 10. A dedicated integrated circuit for performing the software operation having
2 processing elements scheduled according to claim 7.

1 11. The method of forming an application specific reconfigurable circuit,
2 comprising:

3 (a) providing source code for an application to be run b the circuit,

4 (b) deriving flow graphs representing separate portions of the
5 application,

6 (c) identifying at least one largest common flow graph from at least two
7 of the separate portions of the application; and

8 (d) configuring in hardware circuitry to be shared by the separate
9 portions of the application.